CLAIMS

What is claimed is:

1. A binary hysteresis comparator circuit, comprising:

first and second multi-bit circuit input terminals;

a circuit output terminal;

an A-equals-B comparator having a multi-bit A input terminal coupled to the first circuit input terminal, a multi-bit B input terminal coupled to the second circuit input terminal, and an output terminal;

an A-greater-than-B comparator having a multi-bit A input terminal coupled to the first circuit input terminal, a multi-bit B input terminal, and an output terminal;

an A-less-than-B comparator having a multi-bit A input terminal coupled to the first circuit input terminal, a multi-bit B input terminal, and an output terminal;

a logic gate having a first input terminal coupled to the output terminal of the A-greater-than-B comparator, a second input terminal coupled to the output terminal of the A-less-than-B comparator, and an output terminal;

a first multiplexer circuit having a first data input terminal coupled to the output terminal of the A-equals-B comparator, a second data input terminal coupled to the output terminal of the logic gate, a select terminal, and an output terminal;

a memory element having a data input terminal coupled to the output terminal of the first multiplexer circuit, and further having a data output terminal coupled to the circuit output terminal and to the select terminal of the first multiplexer circuit; and

a first hysteresis circuit coupled between the second circuit input terminal and the B input terminal of a first one of the A-greater-than-B comparator and the A-less-than-B comparator.

2. The binary hysteresis comparator circuit of Claim 1, wherein the first hysteresis circuit comprises:

an adder circuit having a multi-bit input terminal coupled to the second circuit input terminal and further having a multi-bit output terminal;

a second multiplexer circuit having a first multi-bit data input terminal coupled to the output terminal of the adder circuit, a second multi-bit data input terminal coupled to the second circuit input terminal, a select terminal, and a multi-bit output terminal coupled to the B input terminal of the first one of the A-greater-than-B comparator and the A-less-than-B comparator; and

an overflow prevention circuit coupled between the second circuit input terminal and the select terminal of the second multiplexer circuit.

3. The binary hysteresis comparator circuit of Claim 2, wherein the first one of the A-greater-than-B comparator and the A-less-than-B comparator comprises the A-greater-than-B comparator, and the adder circuit comprises an adder, wherein the adder adds a first constant to a value on the second circuit input terminal.

4. The binary hysteresis comparator circuit of Claim 3, wherein the first constant is a binary one.

5. The binary hysteresis comparator circuit of Claim 2, wherein the first one of the A-greater-than-B comparator and the A-less-than-B comparator comprises the A-less-than-B comparator, and the adder circuit comprises a subtractor, wherein the subtractor subtracts a second constant from a value on the second circuit input terminal.

6. The binary hysteresis comparator circuit of Claim 5, wherein the second constant is a binary one.

7. The binary hysteresis comparator circuit of Claim 1, wherein the first hysteresis circuit comprises:

a second multiplexer circuit having a first multi-bit data input terminal coupled to receive an all-zero value, a second multi-bit data input terminal coupled to receive a constant, a select terminal, and a multi-bit output terminal;

an adder circuit having a first multi-bit input terminal coupled to the second circuit input terminal, a second multi-bit terminal coupled to the output terminal of the second multiplexer circuit, and a multi-bit output terminal coupled to the B input terminal of the first one of the A-greater-than-B comparator and the A-less-than-B comparator; and

a first overflow prevention circuit coupled between the second circuit input terminal and the select terminal of the second multiplexer circuit.

8. The binary hysteresis comparator circuit of Claim 7, wherein the constant is a binary one.

9. The binary hysteresis comparator circuit of Claim 7, wherein the first one of the A-greater-than-B comparator and the A-less-than-B comparator comprises the A-greater-than-B comparator, and the adder circuit comprises an adder, wherein the adder adds a value provided by the second multiplexer circuit to a value on the second circuit input terminal.

10. The binary hysteresis comparator circuit of Claim 7, wherein the first one of the A-greater-than-B comparator and the A-less-than-B comparator comprises the A-less-than-B comparator, and the adder circuit comprises a subtractor, wherein the subtractor subtracts a value provided by the second multiplexer circuit from a value on the second circuit input terminal.

11. The binary hysteresis comparator circuit of Claim 1, further comprising:

a second hysteresis circuit coupled between the second circuit input terminal and the B input terminal of a second one of the A-greater-than-B comparator and the A-less-than-B comparator.

12. The binary hysteresis comparator circuit of Claim 11, wherein each of the first and second hysteresis circuits comprises:

an adder circuit having a multi-bit input terminal coupled to the second circuit input terminal and further having a multi-bit output terminal;

a second multiplexer circuit having a first multi-bit data input terminal coupled to the output terminal of the adder circuit, a second multi-bit data input terminal coupled to the second circuit input terminal, a select terminal, and a multi-bit output terminal coupled to the B input terminal of one of the A-greater-than-B comparator and the A-less-than-B comparator; and

an overflow prevention circuit coupled between the second circuit input terminal and the select terminal of the second multiplexer circuit.

13. The binary hysteresis comparator circuit of Claim 12, wherein:

in the first hysteresis circuit, the adder circuit is an adder and the output terminal of the second multiplexer circuit is coupled to the B input terminal of the A-greater-than-B comparator, wherein the adder adds a first constant to a value on the second circuit input terminal; and

in the second hysteresis circuit, the adder circuit is a subtractor and the output terminal of the second multiplexer circuit is coupled to the B input terminal of the A-less-than-B comparator, wherein the subtractor subtracts a second constant from the value on the second circuit input terminal.

14. The binary hysteresis comparator circuit of Claim 13, wherein the first and second constants are the same.

15. The binary hysteresis comparator circuit of Claim 14, wherein the first and second constants are both binary ones.

16. The binary hysteresis comparator circuit of Claim 11, wherein each of the first and second hysteresis circuits comprises:

a second multiplexer circuit having a first multi-bit data input terminal coupled to receive an all-zero value, a second multi-bit data input terminal coupled to receive a constant, a select terminal, and a multi-bit output terminal;

an adder circuit having a first multi-bit input terminal coupled to the second circuit input terminal, a second multi-bit terminal coupled to the output terminal of the second multiplexer circuit, and a multi-bit output terminal coupled to the B input terminal of the first one of the A-greater-than-B comparator and the A-less-than-B comparator; and

an overflow prevention circuit coupled between the second circuit input terminal and the select terminal of the second multiplexer circuit.

17. The binary hysteresis comparator circuit of Claim 16, wherein:

in the first hysteresis circuit, the adder circuit is an adder and the output terminal of the adder circuit is coupled to the B input terminal of the A-greater-than-B comparator, wherein the adder adds a value provided by the second multiplexer circuit to a value on the second circuit input terminal; and

in the second hysteresis circuit, the adder circuit is a subtractor and the output terminal of the adder circuit is coupled to the B input terminal of the A-less-than-B comparator, wherein the subtractor subtracts the value provided by the second multiplexer circuit from the value on the second circuit input terminal.

18. The binary hysteresis comparator circuit of Claim 16, wherein in each of the first and second hysteresis circuits the constants are equal.

19. The binary hysteresis comparator circuit of Claim 18, wherein in each of the first and second hysteresis circuits the constant is a binary one.

20. The binary hysteresis comparator circuit of Claim 1, wherein the logic gate is a logical NOR gate.

21. The binary hysteresis comparator circuit of Claim 1, wherein the memory element is a D-type flip-flop.

22. The binary hysteresis comparator circuit of Claim 1, further comprising:

a first multi-bit register coupled between the first circuit input terminal and the A input terminals of the A-equals-B comparator, the A-greater-than-B comparator, and the A-less-than-B comparator, the first register having a clock input terminal; and

a second multi-bit register coupled between the second circuit input terminal and the B input terminals of the A-equals-B comparator, the A-greater-than-B comparator, and the A-less-than-comparator, the second register having a clock input terminal,

wherein the memory element comprises a clock input terminal coupled to the clock input terminals of the first and second registers.

23. The binary hysteresis comparator circuit of Claim 22, further comprising an inverting logic gate coupled between the clock input terminals of the first and second registers and the clock input terminal of the memory element.

24. The binary hysteresis comparator circuit of Claim 22, wherein the first and second registers and the memory element each comprise a reset input terminal, and the reset input terminals of the first and second registers and the memory element are all coupled one to another.

25. A method of performing an equal comparison between first and second binary values while providing binary hysteresis, the method comprising:

reporting, when the first binary value has an initial value not equal to the second binary value, that the first and second binary values are not equal;

reporting, when the first binary value assumes a value equal to the second binary value, that the first and second binary values are equal; and

continuing to report, when the first binary input value assumes a first new value, that the first and second binary values are equal,

wherein the first new value differs from the second binary value by a number not exceeding a predetermined constant.

26. The method of Claim 25, wherein the first new value is greater than the second binary value by the number.

27. The method of Claim 25, wherein the first new value is less than the second binary value by the number.

28. The method of Claim 25, further comprising:

reporting, when the first binary value assumes a second new value differing from the second binary value by a number exceeding the predetermined constant, that the first and second binary values are not equal.

29. The method of Claim 25, wherein the predetermined constant is a binary one.

30. A binary hysteresis comparator circuit performing an equal comparison between first and second binary values while providing binary hysteresis, the circuit comprising:

means for reporting, when the first binary value has an initial value not equal to the second binary value, that the first and second binary values are not equal;

means for reporting, when the first binary value assumes a value equal to the second binary value, that the first and second binary values are equal; and

means for continuing to report, when the first binary input value assumes a new value, that the first and second binary values are equal,

wherein the new value differs from the second binary value by a number not exceeding a predetermined constant.

31. The circuit of Claim 30, wherein the new value is greater than the second binary value by the number.

32. The circuit of Claim 30, wherein the new value is less than the second binary value by the number.

33. The circuit of Claim 30, wherein the predetermined constant is a binary one.

34. A method of performing an equal comparison between first and second binary values while providing binary hysteresis, the method comprising:

reporting, when the first binary value has an initial value not equal to the second binary value, that the first and second binary values are not equal;

reporting, when the first binary value assumes a value equal to the second binary value, that the first and second binary values are equal;

continuing to report, when the first binary input value increases to a first new value, that the first and second binary values are equal, wherein the first new value is greater than the second binary value by a first number not exceeding a first predetermined constant; and

continuing to report, when the first binary input value decreases to a second new value, that the first and second binary values are equal, wherein the second new value is less than the second binary value by a second number not exceeding a second predetermined constant.

35. The method of Claim 34, wherein the first and second predetermined constants are the same.

36. The method of Claim 35, wherein the first and second predetermined constants are binary ones.

37. The method of Claim 34, further comprising:

reporting, when the first binary input value increases to a third new value greater than the second binary value by a third number exceeding the first predetermined constant, that the first and second binary values are not equal.

38. The method of Claim 34, further comprising:

reporting, when the first binary input value decreases to a fourth new value less than the second binary value by a fourth number exceeding the second predetermined constant, that the first and second binary values are not equal.

39. A binary hysteresis comparator circuit performing an equal comparison between first and second binary values while providing binary hysteresis, the circuit comprising:

means for reporting, when the first binary value has an initial value not equal to the second binary value, that the first and second binary values are not equal;

means for reporting, when the first binary value assumes a value equal to the second binary value, that the first and second binary values are equal;

means for continuing to report, when the first binary input value increases to a first new value, that the first and second binary values are equal, wherein the first new value is greater than the second binary value by a first number not exceeding a first predetermined constant; and

means for continuing to report, when the first binary input value decreases to a second new value, that the first and second binary values are equal, wherein the second new value is less than the second binary value by a second number not exceeding a second predetermined constant.

40. The circuit of Claim 39, wherein the first and second predetermined constants are the same.

41. The circuit of Claim 40, wherein the first and second predetermined constants are binary ones.